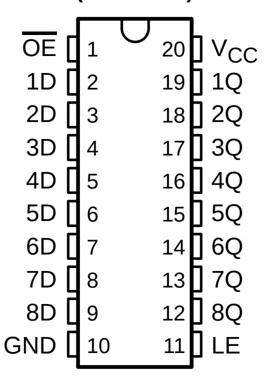
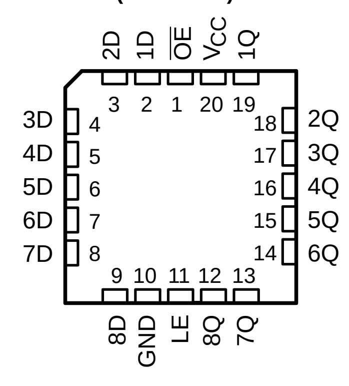
- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**

SN54HC573A . . . J OR W PACKAGE
SN74HC573A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HC573A . . . FK PACKAGE
(TOP VIEW)



description

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

ORDERING INFORMATION

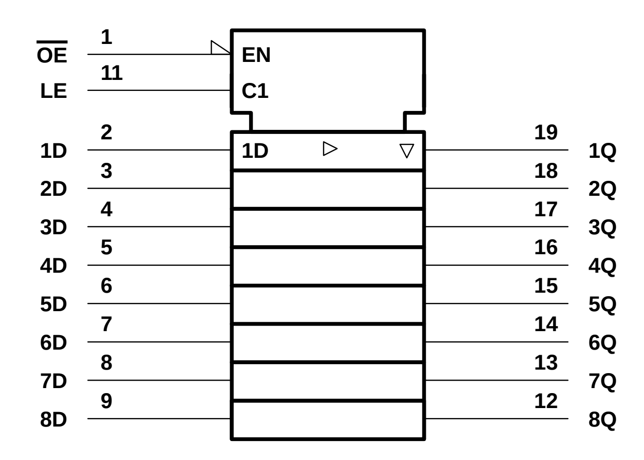
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74HC573AN	SN74HC573AN
	SOIC – DW	Tube	SN74HC573ADW	HC573A
		Tape and reel	SN74HC573ADWR	
	SSOP – DB	Tape and reel	SN74HC573ADBR	HC573A
	TSSOP – PW	Tape and reel	SN74HC573APWR	HC573A
–55°C to 125°C	CDIP – J	Tube	SNJ54HC573AJ	SNJ54HC573AJ
	CFP – W	Tube	SNJ54HC573AW	SNJ54HC573AW
	LCCC - FK	Tube	SNJ54HC573AFK	SNJ54HC573AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each latch)

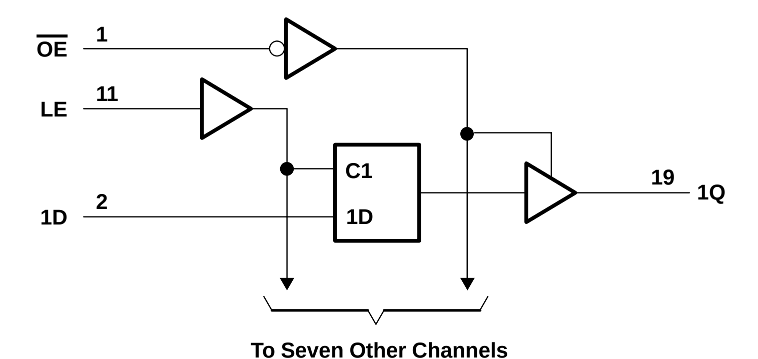
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . 70°C/W
DW package . . . . 58°C/W
N package . . . . 69°C/W
PW package . . . . 83°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			SN54HC573A			SN74HC573A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC573A		SN74HC573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10		±5	µA
I_{CC}	$V_I = V_{CC}$ or 0,	$I_O = 0$	6 V			8		160		80	µA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC573A		SN74HC573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before LE↓	2 V	50		75		63		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data after LE↓	2 V	20		24		24		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54HC573A MIN	SN54HC573A MAX	SN74HC573A MIN	SN74HC573A MAX	UNIT
t_{pd}	D	Q	2 V		77	175		265		220	ns
			4.5 V		26	35		53		44	
			6 V		23	30		45		38	
	LE	Any Q	2 V		87	175		265		220	
			4.5 V		27	35		53		44	
			6 V		23	30		45		38	
t_{en}	$\overline{OE}$	Any Q	2 V		68	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		21	26		38		32	
t_{dis}	$\overline{OE}$	Any Q	2 V		47	150		225		190	ns
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

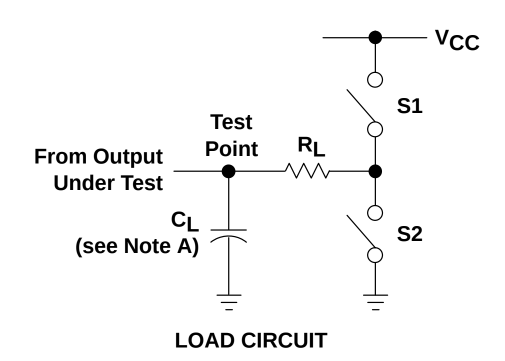
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54HC573A MIN	SN54HC573A MAX	SN74HC573A MIN	SN74HC573A MAX	UNIT
t_{pd}	D	Q	2 V		95	200		300		250	ns
			4.5 V		33	40		60		50	
			6 V		21	34		51		43	
	LE	Any Q	2 V		103	225		335		285	
			4.5 V		33	45		67		57	
			6 V		29	38		57		48	
t_{en}	$\overline{OE}$	Any Q	2 V		85	200		300		250	ns
			4.5 V		29	40		60		50	
			6 V		26	34		51		43	
t_t		Any Q	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

operating characteristics, T_A = 25°C

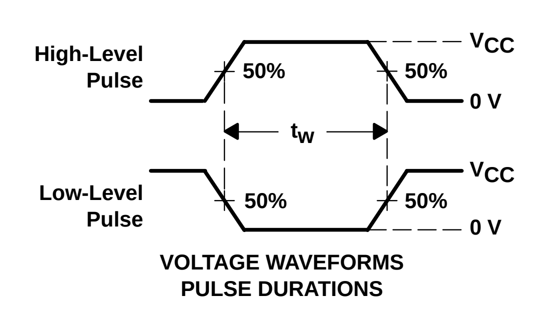
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	No load	50	pF

PARAMETER MEASUREMENT INFORMATION

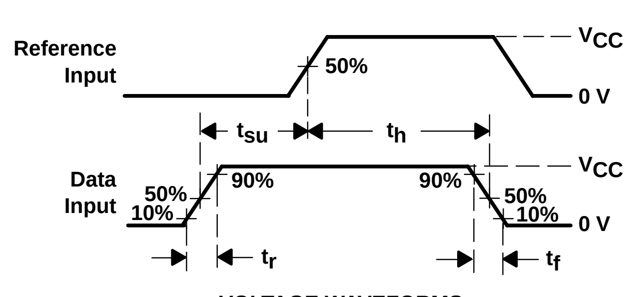


LOAD CIRCUIT

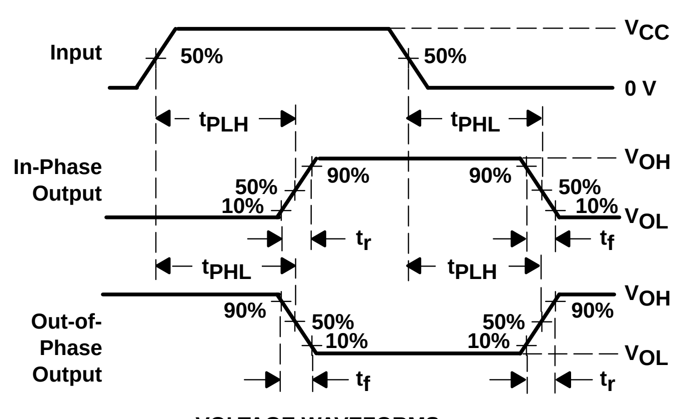
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		––	50 pF or 150 pF	Open	Open



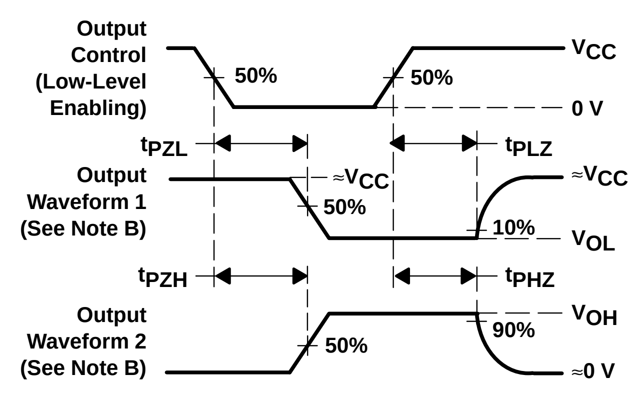
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES:
A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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